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| EXAMINER | |
|---|---|
| HILTUNEN, THOMAS J | |
| **ART UNIT** | **PAPER NUMBER** |
| 2816 | |

DATE MAILED: 09/14/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/823,291 | SUZUKI, HIDEHIKO | |
| | Examiner | Art Unit | |
| | Thomas J. Hiltunen | 2816 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☐ Responsive to communication(s) filed on _____.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-16 and 18-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *23* is/are allowed.

6)☒ Claim(s) *1-22, and 24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

### *Claim Rejections - 35 USC § 112*

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 21-22, and 24 rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

With respect to claims 21, and 22, VDD is not given an explicit definition, and it can be given any arbitrary value. Therefore the scope of the claims is unascertainable. Additionally, there is no antecedent basis for "the first current" in claim 21 on line one of page 6.

With respect to claim 24 the recited language of "the current", on lines 2-3 of page 7, lacks antecedent basis. With respect to the last line of claim 24, it is misdescriptive to state a connection between to elements is made through a ground connection. (i.e. "and the source of the n-type transistor is coupled to the second node"). All of applicant's figures disclose the source of the n-type transistor being connected to a ground line. The voltage at ground is 0V therefore there can be no connection between two elements at ground.

### *Claim Rejections - 35 USC § 102*

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-20, 22, and 24 are rejected under 35 U.S.C. 102(b) as being anticipated by Kong et al. (USPN 6,242,973).

With respect to claim 1, Kong et al. discloses, in Fig.2, a circuit comprising: "a logic circuit (M1 and M2) including a p-type transistor (M1) and an n-type transistor (M2)"; and "a voltage offset circuit (remainder of circuit) that is arranged to provide a first voltage to a gate of the p-type transistor, and further arranged to provide a second voltage to a gate of the n-type transistor such that the second voltage is positively offset relative to the first voltage (Kong et al. discloses a voltage offset through using bootstrap capacitors Cp and Cn. First the capacitor Cp and Cn create a boosted effective control signal opposite in polarity. Additionally in both situations of a high or low input (IN) voltage, M2's gate voltage is positively offset to that of M1's. (See Kong et al. col.2 lines 15-67 and col. 3 lines 1-30.)); and such that, at a voltage threshold of the logic circuit, a source-to-gate voltage of the p-type transistor is greater than a mid-supply voltage of the logic circuit, and the gate-to-source voltage of the n-type transistor is greater than the mid-supply voltage." It can be seen that the p-type's (M1), do to the bootstrapping ability of circuit 100, the source to gate voltage is higher than the mid-supply voltage. When there is a low signal input to it, the gate-to-source voltage is about VDD. VDD is twice that of the mid-supply voltage. Thus it is greater. This bootstrapping function also makes n-type transistor (M2) greater than its gate-to-source voltage. Therefore claim 1 remains rejected, and the rejections for unamended

dependent claims remain.

With respect to claim 2, "the logic circuit is arranged as an inverter circuit (element 11 of Fig.2)".

With respect to claim 3, Kong et al. discloses in Fig. 2, "a logic circuit (M1 and M2) including a p-type transistor (M1) and an n-type transistor (M2)"; and "a voltage offset circuit (remainder of circuit) that is arranged to provide a first voltage to a gate of the p-type transistor, and further arranged to provide a second voltage to a gate of the n-type transistor such that the second voltage is positively offset relative to the first voltage (Kong et al. discloses a voltage offset through using bootstrap capacitors Cp and Cn. First the capacitor Cp and Cn create a boosted effective control signal opposite in polarity. Additionally in both situations of a high or low input (IN) voltage, M2's gate voltage is positively offset to that of M1's. (See Kong et al. col.2 lines 15-67 and col. 3 lines 1-30.)), wherein the voltage offset circuit includes a resistor circuit (it is reasonable to interpret capacitors Cp and Cn, or even transistors M4 or M7 in circuit 10 as a resistor circuit, see "Response to Arguments")."

With respect to claim 4, the capacitors Cp and Cn are arranged serially.

With respect to claim 5, the recited "capacitor circuit" would read on capacitors Cp and Cn.

With respect to claim 6, capacitors Cp and Cn are serially connected.

With respect to claim 7, the bootstrapped configuration of Cp and Cn in Fig. 2 creates a larger effective supply voltage.

With respect to claim 8, the increase in "operation speed" discussed in lines 21-

30 of col. 1 of Kong et al. will inherently provide the recited operation of reduced propagation delay.

With respect to claim 9, transistors M3 and M8, being connected to a supply voltage and ground, clearly provide a current source for circuit 10.

With respect to claim 10, it is well know in the art that the switching of current through a capacitor causes a voltage ramp. This is situation is disclosed in Kong et al., when the voltage supply changes from a high to low value. This causes capacitor Cp in Fig. 2 to become a voltage ramp that differs from the voltage ramp that would occur in Cn, as they would be opposite in magnitude.

With respect to claim 11, Kong et al. discloses in Fig. 2 a circuit comprising:

"a time circuit that is arranged such that(Cp and Cn) circuit, a voltage offset circuit (Cp and Cn in conjunction with M3, M8 and INV) when the timing circuit is activated, an output voltage is asserted after a pre-determined threshold time plus the propagation delay, wherein the pre-determined threshold time is greater than zero, (capacitors Cp and Cn take time to charge. Thus the output of inverter 11 is asserted after the capacitors fully charge and discharge their voltage after a predetermined threshold time (determined by capacitor value (i.e. charge time)), plus the propagation delay (transistors M1 and M2 provide a propagation delay). It is well known that capacitors don't charge and discharge instantaneously. Thus the threshold time is greater than zero), and wherein the timer circuit includes:

a current source circuit that is configured to provide a current (M3 and M8);

a capacitor circuit that is configured to provide a first voltage in response to the

current (capacitors Cp and Cn);

a voltage offset circuit that is coupled between the current circuit and the capacitor circuit, wherein the voltage offset circuit is arranged to provide a second voltage in response to the first voltage and the current such that the second voltage is positively offset relative to the first voltage (capacitors Cp and Cn in conjunction with transistors M3 and M8), and an inverter circuit that includes a p-type transistor and an n-type transistor...(M1 and M2 in Circuit 11)".

With respect to claim 12, Kong et al. discloses in Fig. 2, a circuit comprising:

a current source circuit that is configured to provide a current (M3 and M8);

a capacitor circuit that is configured to provide a first voltage in response to the current (capacitors Cp and Cn);

a voltage offset circuit that is coupled between the current circuit and the capacitor circuit, wherein the voltage offset circuit is arranged to provide a second voltage in response to the first voltage and the current such that the second voltage is positively offset relative to the first voltage (capacitors Cp and Cn in conjunction with transistors M3 and M8), and an inverter circuit that includes a p-type transistor and an n-type transistor...(M1 and M2 in Circuit 11), wherein the voltage offset circuit includes a resistor circuit (the transistors and the capacitors of Kong et al. Fig. 2 can be read as a "resistor circuit" see the rejection for claim 3)."

With respect to claim 13, the recited "capacitor circuit" would read on capacitors Cp and Cn.

With respect to claim 14, "the capacitive circuit enables an effective supply

voltage that is greater than a relatively smaller supply voltage (the bootstrapped configuration of Cp and Cn in Fig. 2 creates a larger effective supply voltage)."

With respect to claim 15, the increase in "operation speed" discussed in lines 21-30 of col. 1 of Kong et al. will inherently provide the recited operation of reduced propagation delay.

With respect to claim 16, it is well know in the art that the switching of current through a capacitor causes a voltage ramp. This is situation is disclosed in Kong et al., when the voltage supply changes from a high to low value. This causes capacitor Cp in Fig. 2 to become a voltage ramp that differs from the voltage ramp that would occur in Cn, as they would be opposite in magnitude.

With respect to claim 18, Kong et al. discloses in Fig. 2, a circuit comprising:

"a logic circuit (11) including a p-type transistor (M1) and an n-type transistor (M2), wherein a drain of the p- type transistor is coupled to a drain of the n-type transistor (M1 and M2 are connected at the drains at the node OUT), and wherein the logic circuit is coupled between a low power supply and a high power supply (11 is coupled between Vdd and ground); and

a voltage offset circuit that is arranged to provide a first voltage to a gate of the p-type transistor (the circuit of M5, M4, M3, Cp, INV, and the input signal IN provide a voltage at the p-type transistor M1), and further arranged to provide a second voltage to a gate of the n-type transistor such that the second voltage (the circuit of M6, M7, M8, Cn, INV, and the input signal IN provide a voltage at the n-type transistor M2), is positively offset relative to the first voltage (for the circuit to properly function a high

(positive voltage signal) must be input into M2, and a low (0 or less voltage signal) must be present at the gate of M1), wherein the positive offset is less than the difference between the high power supply and the low power supply (it can be seen that Cn is and the other transistors of second voltage signal circuit create voltage drops. Thus these drops would cause the positive offset to be "less than the difference between the high power supply and the low power supply)."

With respect to claim 19, Kong et al., discloses in Fig. 2, a circuit comprising:

"a logic (11) circuit including a p-type transistor (M1) and an n-type transistor (M2), wherein a drain of the p- type transistor is coupled to a drain of the n-type transistor (the drains of M1 and M2 are connected at the node OUT), and wherein the logic circuit is coupled between a low power supply (Vss) and a high power supply (Vdd); and

a voltage offset circuit that is arranged to provide a first voltage to a gate of the p-type transistor (the circuit of M5, M3, M4, Cp, INV, and the input signal IN provide a voltage at the n-type transistor M1), and further arranged to provide a second voltage to a gate of the n-type transistor(the circuit of M6, M7, M8, Cn, INV, and the input signal IN provide a voltage at the n-type transistor M2), wherein the voltage offset circuit is operable to provide the first and second voltages such that the logic circuit performs as if the difference between the high power supply and the low power supply was greater than the actual difference between the high power supply and the low power supply (The bootstrapping function of Kong et al. is used to specifically boost the difference in power supply, so that it will be high than the actual difference. Thus the claim is

rejected. See Col. 2 lines 23-27 it states that Cp and Cn are used for "boosting" nodes bnn and bpp. These nodes input the boosted voltage levels to transistor M1 and M2. Thus it can be seen the difference in the voltage levels are greater (boosted))."

With respect to claim 20, Kong et al., discloses in Fig. 2, "the circuit of 19, wherein the low power supply is ground (Vss), and the high power supply is VDD (Vdd on the sources of M1 and M3))."

With respect to claim 22, Kong et al., discloses in Fig. 2, "the circuit of claim 20, wherein the voltage offset circuit is operable to provide the first and second voltages such that the logic circuit performs as if the difference between the high power supply and low power supply was approximately 3*VDD/2. Since, the value of VDD is not explicitly defined it can be defined as any voltage. Therefore Kong et al.'s circuit discloses the circuit in that any voltage within in the circuit could by 3/2 of some arbitrary voltage.

With respect to claim 24, Kong et al., discloses in Fig. 2, "a circuit comprising:

a current source circuit having at least an output that is coupled to a first node (M8 is a current source with an output coupled to a first node (bnn);

a capacitor circuit (Cp) that is coupled between a second node (N1) and a third node (bpp), wherein the second node is coupled to ground (Through Cn, through M7, and finally M8 to ground), and wherein the capacitor circuit is operable to provide a first voltage at the third node (the voltage at bp will get pulled up through M4 and then go to bpp when IN is high);

a voltage offset circuit that is coupled between the first node and the third node

(Cp and Cn are a voltage offset coupled between bpp (through M4) and bnn (through M7)), wherein the voltage offset circuit is operable to provide a second voltage (voltage at bnn) in response to the first voltage and a current such that the second voltage is positively offset relative to the first voltage (for the inverter 11 to output a low (bnn must be higher than bpp); and an inverter circuit that includes:

a p-type transistor having at least a gate, a drain, and a source, (M1 has a gate drain and source) wherein the gate of the p-type transistor is coupled to the third node (the gate is coupled to bpp), the drain of the p-type transistor is coupled to a fourth node (the node connect to OUT), and the source of the p-type transistor is coupled to a fifth node; the fifth node is a power supply node (The drain is connected to power (Vdd)); and wherein, regardless of the logic level at the gate of the p-type transistor, the capacitor circuit is coupled between the gate of the p-type transistor and the second node; (The capacitor circuit Cp is always physically coupled to M1 through the drain of M5, and the source of M4. The coupled means a physical connection, not an operable connection) and

an n-type transistor having at least a gate, a drain, and a source, (M2 has a gate drain and source) wherein the gate of the n-type transistor is coupled to the first node (the gate is coupled to bnn the first node), the drain of the n-type transistor is coupled to the fourth node (the drain of M2 is connected to the OUT node), and the source of the n-type transistor is coupled to the second node.

***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 21 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kong et al. (USPN 6,242,973) in view of Sanwo et al. (USPN 6,472,906).

Kong et al. teaches the circuit of claim 19 (see rejection of claim 19). What Kong et al. fails to disclose is a circuit wherein "the offset voltage includes a resistor" (resistive circuit is broad enough to read on a capacitor. However, a capacitor is not single "resistor" element.) However, Sanwo et al. discloses a driver (inverter) (60) that has a resistor being used as a pull-up device (R2, see Col. 5 lines 33-35). This driver circuit (60) is shown to be used as an inverter (element 60 of Fig. 2 a-c all show it being used as inverter, see "BRIEF DESCRIPTION OF THE DRAWINGS" for Fig. 5). The advantage of using this inverter is that it saves power by not having to use a PFET to hold the current of the NFET. Therefore it would be obvious to one skilled in the art at the time of the invention to use Sanwo et al.'s generic inverter in place of Kong et al.'s generic inverter (INV) of fig. 2. One would be motivated to do this, because of Sanwo et al.'s inverter's ability to save power. With the above modification a resistor would be included in the voltage offset circuit (R2 of Sanwo et al. the inverter INV was part of the voltage offset circuit.). Also, the differences in the first and second voltages could be VDD+I1*R1 (R1 being R2 of Sanwo et al.), because VDD is an arbitrary value that could

be anything.

***Response to Arguments***

With respect to claims 1, 2, and 5-10, examiner finds applicant's arguments unpersuasive. The added language of, "a source-to-gate voltage of the p-type transistor is greater than a mid-supply voltage of the logic circuit, and the gate-to-source voltage of the n-type transistor is greater than the mid-supply voltage", is disclosed by Kong et al (see rejection for claim 1). It can be seen that because of Kong et al.'s bootstrapping abilities (from capacitors Cp and Cn), the source to gate voltage (at bpp) of the p-type transistor (M1) is about full supply voltage (Vdd). Mid-supply voltage is Vdd/2, and Vdd is larger than Vdd/2 (this situation also holds for the n-type (M2) transistor at bnn). Kong et al. discloses the added recitation, therefore claim 1 remains rejected as well as its unamended dependent claims (claims 2, and 5-10).

With respect to claims 3, 4, and 12, examiner finds applicant's arguments unpersuasive. First, the resistive circuit can also read on a transistor. Additionally, it is noted that a capacitor does read on applicant's definition of a resistor, "a resistor is a piece of material that obeys Ohm's Law." It is well know that all circuit elements obey Ohm's Law, including capacitors. The definition of Ohm's Law according to is "many materials contain some 'free' electrons which can move in response to an applied electric field. By attaching a pair of metal wires and applying a voltage between them we can move these charge carriers through the material. The result is a current whose magnitude depends on the characteristics of the piece of material and the applied voltage." (LESURF, JIM. The Scots Guide to Electronics. University of St. Andrews, St.

Andrews, Fife KY16 9SS, Scotland. [online], December 29, 2002 [retrieved on 2005-09-01]. Retrieved from the Internet:< URL: http://www.standrews.ac.uk/~www_pa/Scots_Guide/info/comp/passive/resistor/ohms_law/ohms_law.htm>). Capacitors have a wire that voltage can be applied to, which will result in a current "whose magnitude depends on the characteristics (resistivity, length, cross sectional area, etc.)" of the capacitor. Thus a capacitor obeys Ohm's law, and according to applicant's definition is a "resistor". It is also noted that applicant did not claim a "resistor", but a "resistor circuit". The broadest reasonable interpretation of a "resistor circuit" would be a circuit that provides a resistance. It is well know that a capacitor provides resistance. Markarian (USPN 4,231,07) discloses a "tantalum foil capacitor with a low equivalent series *resistance* (see col.1 lines 27-28)." Therefore a capacitor in its broadest reasonable interpretation can be a "resistive circuit". Also, it is well known that in the AC impedance is the same as DC resistance, in that both impedance (in AC circuits) and resistance (in DC circuits) restrict the flow of current. Thus, in AC circuits a capacitor essential performs the same function as a resistor. Claim 12 is rejected based on reasons similar to claim 3. Claim 4 has not been amended to change its previous scope, thus its pervious rejection still holds.

With respect to claims 11 and 13-16, examiner finds applicant's arguments unpersuasive. Kong et al does disclose a "timer circuit", which has "a capacitor (Cp and Cn) circuit, a voltage offset circuit (Cp and Cn in conjunction with M3 and M8), an inverter circuit (11), and a current source (M3 and M8)". These components act as "a timer circuit" according to applicant's recitation, because capacitors take time to charge.

Thus the output of inverter 11 is asserted after the capacitors fully charge and discharge their voltage after a predetermined threshold time (determined by capacitor value (i.e. charge time)) plus the propagation delay (transistors M1 and M2 provide a propagation delay). It is well known that capacitors don't charge and discharge instantaneously. Thus it is obvious that Kong et al.'s threshold time is greater than zero. Since newly amended claim 11 does add any patentable weight to the original claim 11, the rejection for claims 11, and 13-16 still hold.

It should be noted that the publish date of the Lesurf website reference was found by using the website archive.org <URL: http://www.archive.org> [access date 2005-09-31]. The following web address will give the results of dates published for the Lesurf website <URL: http://web.archive.org/web/*/http://www.st-andrews.ac.uk/~www_pa/Scots_Guide/info/comp/passive/resistor/ohms_law/ohms_law.htm> [date accessed 2005-09-01]. This website shows the oldest publishing date of reference's website is December, 29 2002. By selecting the link provided by the date the following website was accessed on September, 1 2005 <URL: http://web.archive.org/web/20030308223459/www.st-andrews.ac.uk/~www_pa/Scots_Guide/info/comp/passive/resistor/ohms_law/ohms_law.htm This website displays a definition of Ohm's Law in accordance with definition found by accessing the page on September, 1st 2005. Thus, it can be seen that the information provide by accessing the website < URL: http://www.st-andrews.ac.uk/~www_pa/Scots_Guide/info/comp/passive/resistor/ohms_law/ohms_law.htm>, was available as early as December 29, 2002.

### *Allowable Subject Matter*

With respect to claim 23, the examiner agrees with applicant that Kong et al. does not teach a current mirror. Also, a circuit that teaches the use of a current mirror to output a current to a capacitor circuit that "provides a first voltage" in the updated search. There was also no references found that provides motivation for the combination of the circuit of claim 23 with a current mirror.

### *Conclusion*

**THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thomas J. Hiltunen whose telephone number is (571) 272-5525. The examiner can normally be reached on Mondays - Fridays from 8:00am

to 4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy P. Callahan, can be reached on (571) 272-1740. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

**Terry D. Cunningham**
**Primary Examiner**
**Art Unit 2816**

**TH**
**September 6, 2005**